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Review Article

Formation and Device Application of Ge Nanowire Heterostructures via Rapid Thermal Annealing

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We reviewed the formation of Ge nanowire heterostructure and its field-effect characteristics by a controlled reaction between a single-crystalline Ge nanowire and Ni contact pads using a facile rapid thermal annealing process. Scanning electron microscopy and transmission electron microscopy demonstrated a wide temperature range of 400∼500°C to convert the Ge nanowire to a single-crystalline $Ni_2Ge/Ge/Ni_2Ge$ nanowire heterostructure with atomically sharp interfaces. More importantly, we studied the effect of oxide confinement during the formation of nickel germanides in a Ge nanowire. In contrast to the formation of $Ni_2Ge/Ge/Ni_2Ge$ nanowire heterostructures, a segment of high-quality epitaxial NiGe was formed between Ni_2Ge with the confinement of Al_2O_3 during annealing. A twisted epitaxial growth mode was observed in both two Ge nanowire heterostructures to accommodate the large lattice mismatch in the Ni_xGe/Ge interface. Moreover, we have demonstrated field-effect transistors using the nickel germanide regions as source/drain contacts to the Ge nanowire channel. Our Ge nanowire transistors have shown a high-performance *p*-type behavior with a high on/off ratio of 10^5 and a field-effect hole mobility of 210 cm^2/Vs, which showed a significant improvement compared with that from unreacted Ge nanowire transistors.

1. Introduction

As an important one-dimensional material, semiconductor nanowire has attracted enormous research interest for its unique electrical properties, which has promising applications as building blocks for nanoelectronics [1–5]. Since 2004, there have been a lot of efforts on studying the thermal diffusion of metal into a single-crystalline Si nanowire, in which a silicide/silicon/silicide nanowire heterostructure is formed by solid-state reactions between the Si nanowire and metal contacts. Many metals (contact pads or nanowires) have been studied as the diffusion source, such as Ni [6–8], Co [9], Pt [10], and Mn [11]. One of the salient features in this nanowire heterostructure is the atomically sharp interface between the Si nanowire and the formed silicide nanowire. Such clean interface may help to avoid Fermi-level pinning effect, which is commonly observed in conventional metal-semiconductor contacts [12]. Also, the nanowire heterostructure can be easily used to fabricate nanowire field-effect transistors (FETs) using the formed silicide regions as the source/drain contacts to the Si nanowire channel [6, 7, 10]. The channel length can be well controlled by the annealing time and growth length of silicide, therefore, can be aggressively shrunk down to sub-50 nm [11]. Clearly, this process offers great advantages over modern high-cost and complex photolithography technology to fabricate short-channel transistors and may further facilitate the advance of scaled nanodevices.

Compared with Si nanowire, metal-Ge nanowire is a new system of interest, since Ge is an important complement to Si with even higher carrier mobilities for further device miniaturization compatible to the existing CMOS technology [1, 2]. For Ge, the atomically sharp interface is of particular interest to alleviate the Fermi-level pinning effect in the metal-Ge contact, since Ge has a high density of interface states due to native defects on the Ge surface [12].

Experimentally, Yamane et al. have demonstrated the epitaxial growth of high-quality Fe_3Si on Ge(111) substrate with an atomically controlled interface, which successfully depined the Fermi-level of Fe_3Si/Ge contact [19]. It is, therefore, highly desirable to achieve a metallic contact to Ge with a high-quality interface. On the other hand, many germanides, such as Mn_5Ge_3 and Ni_3Ge, exhibit ferromagnetism above room temperature [20, 21], and thus offer great advantages over silicides for future applications in spintronics, such as realizing spin injection into semiconductor from a ferromagnetic contact. Therefore, there is an increasing research interest on the metal-Ge nanowire system, such as Ni-Ge [13–15] and Cu-Ge [16–18]. For comparison, Table 1 briefly summarizes the literature report of Si and Ge nanowire heterostructures formed by solid-state reactions between a semiconductor nanowire and metal contacts. It is noted that the annealing temperature of metal-Ge nanowire system is usually lower than that of metal-Si nanowire system, which is partially due to a lower melting point of Ge than Si. The low-temperature process in metal-Ge nanowire systems is favorable to reduce the thermal budget in forming nanowire heterostructures toward future process integration.

In this paper, we will first discuss the formation of single-crystalline Ge nanowire heterostructure by the solid-state reaction between a Ge nanowire and Ni contact pads. By a comparative study of with or without an Al_2O_3 capping layer during annealing, we study the effect of oxide confinement in the growth of germanide in a Ge nanowire. A detailed transmission electron microscopy (TEM) analysis including the epitaxial relationships is presented in this section. In the second part of this paper, we will introduce electrical characterizations of Ge nanowire back-gate FETs fabricated using the Ge nanowire heterostructures. Specifically, the effect of Al_2O_3 capping layer on the device performance is studied in this section. Finally, we will discuss the possible research directions for future work on the Ge nanowire heterostructures, especially for promising applications in spintronics and further study on the growth dynamics.

2. Experimental Results

The growth of Ge nanowires can be accomplished by a variety of techniques. In this study, two popular methods were employed to synthesize single-crystalline Ge nanowire with ⟨111⟩ growth direction. One is the supercritical fluid-liquid-solid (SFLS) approach, in which Ge nanowires were produced in highly pressurized supercritical fluids enriched with organogermane precursors and metal nanocrystals as catalyst [22, 23]. The typical diameter of as-synthesized Ge nanowires is around 40–50 nm and the length could be more than 10 μm. The other approach is the vapor-liquid-solid (VLS) method, in which metal (such as Au) catalyzed Ge nanowires were grown on SiO_2/Si(100) substrates by means of chemical vapor deposition (CVD) using a gaseous Ge precursor GeH_4 [24]. The VLS-grown Ge nanowires are typically 70–80 nm in diameter and have lengths over 10 μm. The reported carrier mobility of VLS-grown Ge nanowires is higher than SFLS-synthesized Ge nanowires [13, 14], while the latter method is claimed to provide a better control of the nanowire size and a higher product yield [23, 25]. In both two methods, Ge nanowires are not doped on purpose during growth, but unintentional doping usually occurs [26, 27].

To form Ni_xGe/Ge nanowire heterostructures, SFLS-synthesized Ge nanowires diluted in isopropyl alcohol (IPA) were dispersed onto a SiO_2/Si substrate. The top thermal SiO_2 was about 330 nm thick. The Si substrate was degenerately doped with a resistivity of 1–5 $\times 10^{-3}$ Ω-cm, which served as a back gate for further device characterization. E-beam lithography (EBL) was used to define Ni contacts to Ge nanowires. Before e-beam evaporation of about 120 nm-thick Ni (with the purity of 99.995% and in vacuum at a pressure lower than 10^{-6} Torr), the sample was dipped into diluted hydrofluoric acid (HF) for 15 s to completely remove native oxide in the contact region. A field-emission scanning electron microscopy (JEOL JSM-6700 FESEM) was used to examine the sample morphology before and after the annealing process. Figures 1(a) and 1(b) show the device schematics before and after the thermal diffusion of Ni into the Ge nanowire. Figure 1(c) shows the SEM image of the as-fabricated Ge nanowire device showing a uniform contrast. Then the sample was annealed with rapid thermal annealing (RTA) in the ambient of N_2 to allow Ni thermal intrusion into Ge nanowire and subsequently form Ni_xGe/Ge heterostructures along the nanowire. In the previous study on the interfacial reactions of Ni thin film on Ge(111) substrate, the germanide phase formation sequence was found to be Ni_2Ge and NiGe at increasing temperatures in the range of 160°C to 600°C [28]. Various annealing temperatures ranging from 400°C to 700°C were used in this study to optimize the formation of nanowire heterostructures. It is found out that Ge nanowires were easily broken at a high annealing temperature (>550°C) due to the significant reduction of the melting point for Ge nanowires compared with that of bulk Ge [29]. When the temperature decreased to 400°C–500°C, clear diffusion of Ni into the Ge nanowire was also observed and the formed germanide was identified to be Ni_2Ge (refer to the TEM analysis later). Figure 1(d) shows the SEM image of the Ge nanowire device upon RTA at 500°C for 60 s, in which clear contrast was observed between the Ge nanowire and the formed nickel germanide nanowire due to the conductivity difference. The remained Ge region was easily controlled down to 650 nm, and it can be further reduced to sub-100 nm [11, 16]. Similar contrast was also observed after RTA at 400°C for 40 s, as shown in Figure 1(e).

In order to identify the phase of the formed germanide and the epitaxial relationship of germanide-germanium interface, *in situ* TEM was used to study the formation process and reaction kinetics. To prepare the TEM sample, the single-crystalline Ge nanowires were dispersed on the TEM grid with a square opening of a Si_3N_4 thin film. The low-stress Si_3N_4 film was deposited by low-pressure chemical vapor deposition (LPCVD). The Si_3N_4 film was about 50 nm thick, which provided a reliable mechanical support for Ge nanowire devices during the fabrication process and at the same time to assure it is transparent to the electron

Table 1: Summary of Si and Ge nanowire heterostructures formed by solid-state reactions between a semiconductor nanowire and metal contacts.

Material system	Annealing condition (°C)	Formed silicide/germanide	Metal diffusion source
Ni-Si [6]	550	NiSi	Ni contact pad
Ni-Si [7]	470	$NiSi_x$ (not identified)	Ni contact pad
Ni-Si [8]	500–700	NiSi	Ni nanowire
Co-Si [9]	700	CoSi	Co nanodots
	800	Co_2Si	Co nanodots
Pt-Si [10]	520	PtSi	Pt contact pad
Mn-Si [11]	650	MnSi	Mn contact pad
Ni-Ge [13]	400–500	Ni_2Ge	Ni contact pad
Ni-Ge [14]	450 (capped with Al_2O_3)	Ni_2Ge/NiGe	Ni contact pad
Ni-Ge [15]	300–450	Ni_2Ge	Ni contact pad
Cu-Ge [16–18]	310	Cu_3Ge	Cu contact pad

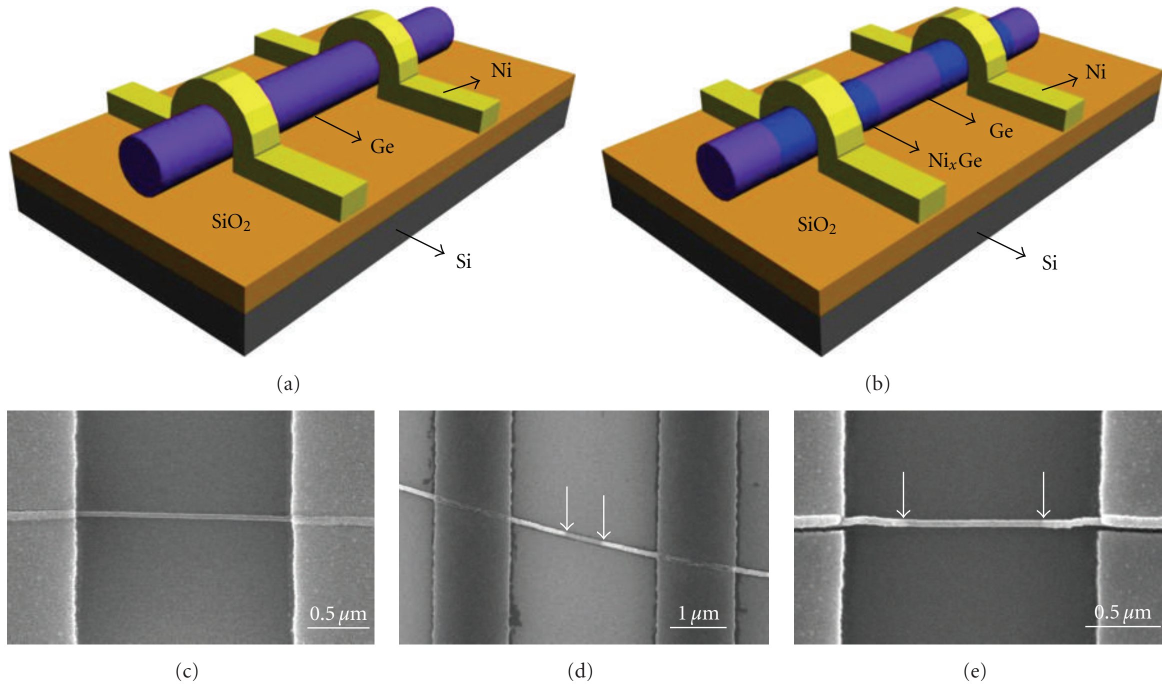

Figure 1: Formation of Ni_2Ge/Ge/Ni_2Ge heterostructures. Schematic illustration showing (a) before and (b) after the diffusion process of Ni into the Ge nanowire forming a Ni_2Ge/Ge/Ni_2Ge heterostructure. (c) SEM image of the Ge nanowire device with EBL defined Ni electrodes. (d) SEM image of the Ni_2Ge/Ge/Ni_2Ge heterostructure after RTA at 500°C for 60 s in which the length of the Ge region was easily controlled to submicron range. The arrows indicate the growth tips of the Ni_2Ge nanowire. (e) SEM image of the Ni_2Ge/Ge/Ni_2Ge heterostructure after RTA at 400°C for 40 s. The arrows indicate the growth tips of the Ni_2Ge nanowire. Reproduced from [13].

beam without interference with images of the nanowires. EBL-defined Ni pads were employed as the Ni diffusion source. A JEOL-2010 TEM (operated at 200 KV with a point-to-point resolution of 0.25 nm) attached with an energy dispersive spectrometer (EDS) was used to investigate the microstructures and to determine the compositions of the samples. To *in situ* observe the reactions of the Ni electrodes with Ge nanowires, the samples were heated inside TEM with a heating holder (Gatan 652 double tilt heating holder connected with a power supply to heat up the samples to the desired temperature) under a RTA mode with a pressure below 10^{-6} Torr. Figures 2(a)–2(c) show high-resolution TEM (HRTEM) images of the formed Ni_xGe/Ge interface upon 500°C annealing. According to the lattice-resolved HRTEM analysis, the formed germanide was identified to be single-crystalline Ni_2Ge with an orthorhombic lattice structure and lattice constants $a = 0.511$ nm, $b = 0.383$ nm, and $c = 0.726$ nm (space group 62). It was observed that a large lattice mismatch of 56.3% at the Ni_2Ge/Ge epitaxial interface could result in the segregation of nanoparticles (see Figure 4). In Figure 2(b), a clean and sharp interface between Ni_2Ge/Ge was observed with an approximately 1 nm GeO_x

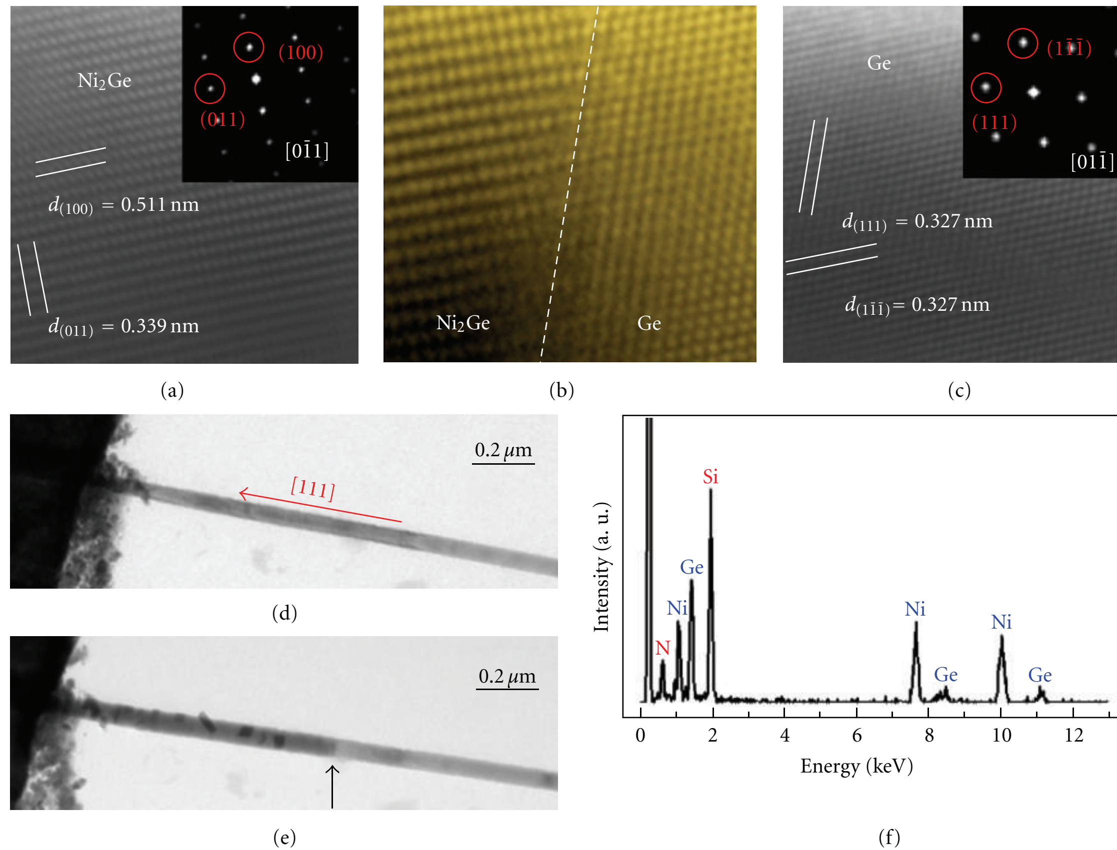

FIGURE 2: Epitaxial relationship at the Ni_2Ge/Ge interface. (a) Lattice-resolved TEM image of the formed Ni_2Ge nanowire. The inset shows the FFT pattern, confirming that the formed germanide phase is Ni_2Ge. (b) TEM image of Ni_2Ge/Ge heterostructure showing an atomically sharp interface. (c) Lattice-resolved TEM image of the unreacted Ge nanowire. The inset shows the FFT pattern. (d) Low magnification TEM image of the as-fabricated device with the Ni pad and the Ge nanowire. (e) Low magnification TEM image after annealing at 500°C. The arrow indicates the interface of the Ni_2Ge/Ge nanowire. (f) EDS of Ni_2Ge, showing a relative 2 : 1 concentration ratio of Ni and Ge atoms. Reproduced from [13].

shell surrounding both the Ge and Ni_2Ge regions. The insets in Figures 2(a) and 2(c) illustrate the fast Fourier transform (FFT) patterns of Ni_2Ge and Ge HRTEM images, respectively. The crystallographic epitaxial relationships between Ge and Ni_2Ge are shown to be Ge$[01\bar{1}]$//$Ni_2Ge$$[0\bar{1}1]$ and Ge$(1\bar{1}\bar{1})$//Ni_2Ge(100), as we discussed. Figures 2(d) and 2(e) show the low-magnification TEM images of Ge NWs before and after annealing at 500°C, respectively. Figure 2(f) shows the EDS of the formed germanide nanowire region, showing that the ratio of Ni to Ge concentration is about 2 : 1, which further support the fact that the formed germanide phase is Ni_2Ge. The signals of Si and N peaks are contributed from the Si_3N_4 window.

Real-time observation on the Ni_2Ge growth in a Ge nanowire was performed using *in situ* TEM video, which allows us to obtain lattice-resolved TEM images of the epitaxial interface in progression and thus to estimate the growth velocity. Figure 3(a) shows the relation of Ni_2Ge nanowire length versus the reaction time at 400 and 500°C, illustrating a potentially linear growth behavior of Ni_2Ge in the Ge nanowires, while the detailed growth mechanism requires further study. Figures 3(b), 3(c), 3(d), and 3(e) show the *in situ* TEM images of the Ni_2Ge nanowire growth at 400 and 500°C, respectively. The growth length of the Ni_2Ge nanowire is 138.9 nm for 455 s at 400°C and 357.5 nm for 340 s at 500°C, respectively. Based on the data collected on more than three nanowires, the extracted growth velocities are about 0.31 nm/s at 400°C and 1.05 nm/s and 500°C, respectively. Using the Arrhenius plot [8], the activation energy of the Ni_2Ge growth in the Ge nanowire is estimated to be 0.55 ± 0.05 eV/atom.

As mentioned above, due to a large lattice mismatch on the Ni_2Ge/Ge epitaxial interface, the resulting huge strain in the Ni_2Ge/Ge/Ni_2Ge nanowire heterostructure could lead to the segregation of Ni_2Ge nanoparticles on the Ni_2Ge nanowire after a long-time annealing. Figure 4(a) shows the TEM image of an as-fabricated Ge nanowire device with EBL-defined Ni pads at room temperature. Figures 4(b)–4(d) are a series of *in situ* TEM images of the Ge nanowire device upon 400°C, 450°C and 500°C sequential annealing, respectively. The time clocks shown at the lower-right corner in each TEM image were captured in the form of hour: minute:second. Volume expansion and segregation to form nanoparticles were clearly observed. Figure 4(e) shows a

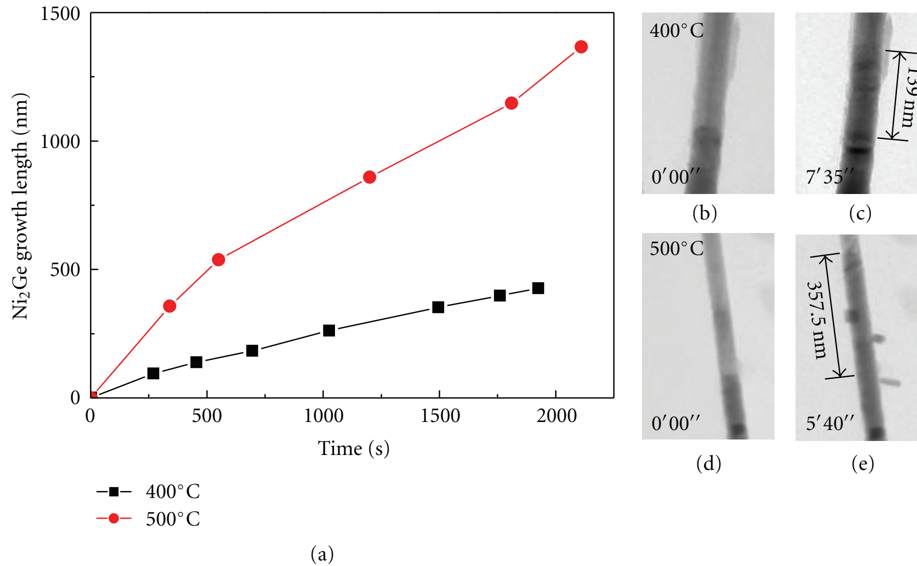

Figure 3: Kinetic analysis of the Ni_2Ge epitaxial growth within Ge nanowires. (a) Real-time record of the Ni_2Ge nanowire growth length versus the reaction time at 400 and 500°C, illustrating a potentially linear growth rate. (b)-(c) *In situ* TEM images of the Ni_2Ge growth within a Ge nanowire at 400°C annealing. The arrow indicates a corresponding length of 138.9 nm growth in 7 min 35 sec. (d)-(e) *In situ* TEM images of the Ni_2Ge growth within a Ge nanowire at 500°C annealing. The arrow indicates a corresponding length of 357.5 nm growth in 5 min 40 sec. Reproduced from [13].

TEM image of another Ge nanowire device annealed at 400°C for 30 min. The results in Figures 4(c)–4(e) clearly demonstrate that as a result of strain release, Ni_2Ge nanoparticles were formed and segregated on the Ni_2Ge nanowire as Ni diffused along the formed Ni_2Ge nanowire.

Similarly, the segregation of nanoparticles during annealing was also observed in the Ni-Si nanowire system as reported by Weber et al. [7]. For Si, a thin layer of high-quality native oxide is usually formed on the Si nanowire surface, while Ge does not have a stable native oxide. It is observed that the SiO_2 shell has a substantial confinement effect on the nickel silicide growth along with phase transformation in a Si nanowire [30]. We studied the effect of oxide confinement on the germanide growth in a Ge nanowire; an oxide layer, such as Al_2O_3, was deposited to cap the Ge nanowire device before the annealing process, as shown in the schematics of Figure 5(a). Figure 5(b) shows the SEM image of the as-fabricated Ge nanowire device showing uniform contrast. Prior to RTA, 20 nm thick Al_2O_3 was deposited on top by atomic layer deposition (ALD) at 250°C (Figure 5(c)). It was noticed that the diameter of the Ge nanowire was increased after the Al_2O_3 deposition since ALD provided a conformal coverage. After that the sample was then annealed with RTA in N_2 ambient to allow for the thermal intrusion of Ni into the Ge nanowire and subsequently form the Ni_xGe/Ge heterostructures along the nanowire. Clear diffusion of Ni into the Ge nanowire was observed in both SEM and TEM, and the formed germanide was analyzed in HRTEM, as to be explained further later. Figure 5(d) shows the SEM image of the Ni_xGe/Ge/Ni_xGe heterostructures after RTA at 450°C for 20 s. Clear contrast was observed between the Ge nanowire and the formed nickel germanide nanowire, which is again attributed to the conductivity difference of the two. Figure 5(e) schematically illustrates the formation of Ni_xGe/Ge/Ni_xGe nanowire heterostructure with the Al_2O_3 confinement. The red line indicates the position where the device was cut with focused ion beam (FIB) to study the cross-sectional structure, as to be explained in Figure 6.

Figure 6(a) shows the low-magnification cross-sectional TEM image of the Ni_xGe/Ge nanowire heterostructure, which was cut with FIB from the Ge nanowire device fabricated on a SiO_2/Si wafer, as shown in Figure 5(e). Before FIB cutting, a 200 nm-thick Pt film was deposited on top to protect the Ni_xGe/Ge/Ni_xGe nanowire heterostructure from the ion beam bombardment. When preparing the cross-section of Ni_xGe for TEM analysis using FIB, we chose the position as close as to the Ni_xGe/Ge interface. It is noted that in the cross-sectional view, there were some nanoparticles segregated on the SiO_2 surface from the bottom of the formed nickel germanide, the region that was not confined by the Al_2O_3 capping layer. This result also explains the fact that we did not observe nanoparticles on the Al_2O_3 capped surface from the SEM image shown in Figure 5(d). Figure 6(b) shows the lattice-resolved HRTEM image of the interface between the formed NiGe nanowire and the segregated NiGe nanoparticle, which were both identified to be NiGe from the FFT pattern shown in the inset of Figure 6(b). NiGe has an orthorhombic lattice structure with lattice constants a = 0.538 nm, b = 0.342 nm, and c = 0.581 nm (space group 62). In order to further confirm the germanide phase, an EDS line scan was performed through

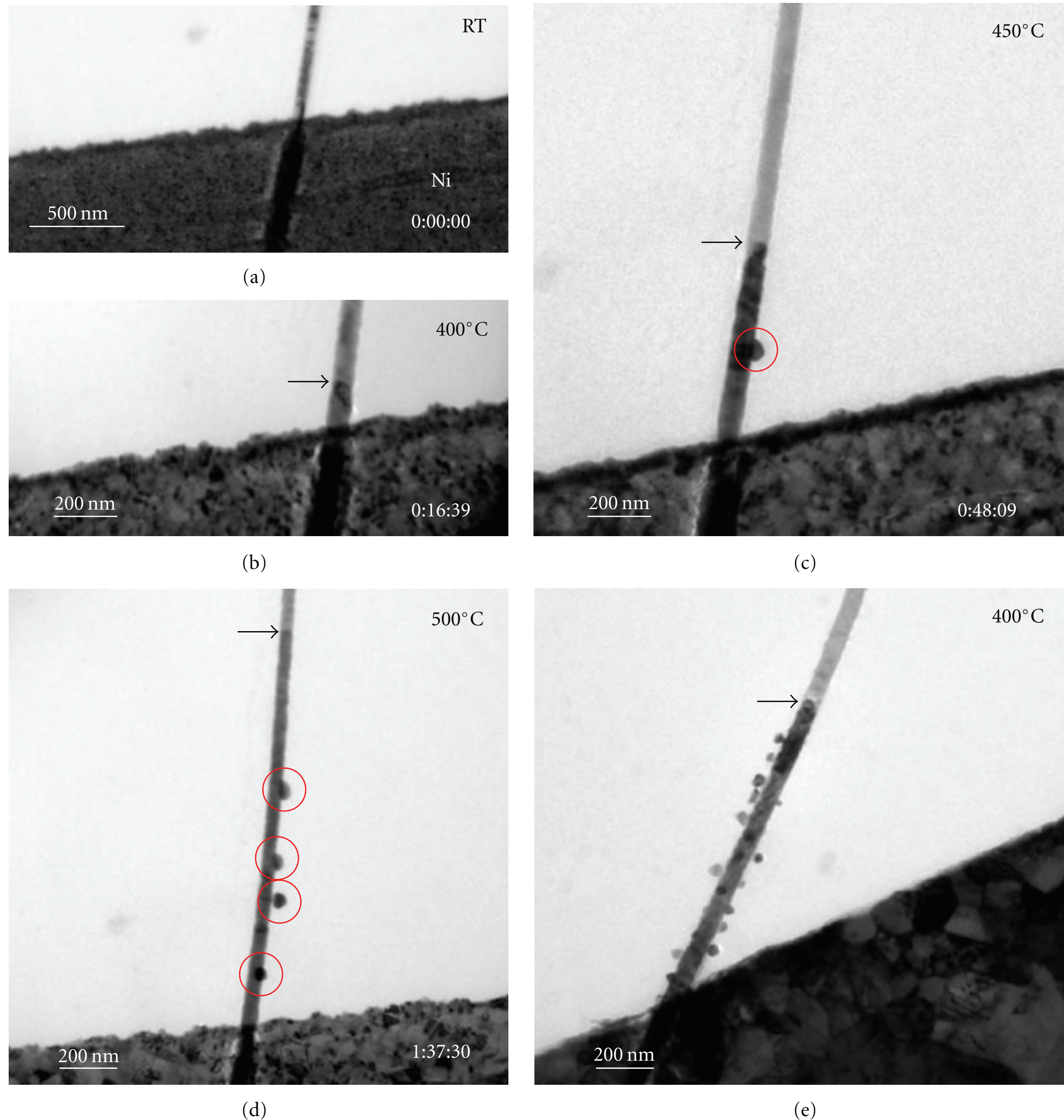

Figure 4: A series of *in situ* TEM images at various annealing temperatures: (a) room temperature; (b) 400°C; (c) 450°C; (d) 500°C. The arrows indicate the interface between the formed Ni_2Ge and the Ge nanowire. The red circles indicate Ni_2Ge nanoparticles segregated from the Ni_2Ge nanowire. (e) TEM image of the Ni electrode reacted with a Ge nanowire upon 400°C annealing for 30 min. Reproduced from [13].

the Al_2O_3-capped Ni_xGe nanowire to determine the profiles of Ge, Ni, Al and O atoms, as shown in the cross-sectional TEM image in Figure 6(c) as well as the individual line-scan profile in Figures 6(d)–6(g). From Figures 6(d) and 6(e), the Ni/Ge ratio was estimated to be about 1 : 1, which further proved the NiGe phase.

To study the epitaxial relationships between Ni_xGe and Ge, the VLS-grown Ge nanowires were dispersed on the TEM grids with a square opening of a Si_3N_4 thin film, as described above. The sample preparation was similar to the process as explained above for the Ni_2Ge/Ge/Ni_2Ge nanowire heterostructure. The only difference is that before the annealing process, an Al_2O_3 film was deposited by ALD at 250°C to cap the device and confine the solid state reaction of germanidation during annealing. The Al_2O_3-coated devices were then annealed both *in situ* (inside TEM) and *ex situ* (in RTA). Figure 7(a) shows the low-magnification TEM image of the Ni-Ge nanowire device capped with 10 nm Al_2O_3 after annealing at 450°C for 30 s. The enlarged TEM image in Figure 7(b) shows that there are clearly two interfaces in the Ni_xGe/Ge nanowire heterostructure. Figure 7(c) shows the EDS line-scan profile from the nanowire heterostructure. The line profile indicates two germanide phases in the formed Ni_xGe region, which corresponds to the two interfaces observed in the Ni_xGe/Ge heterostructure. The Ni/Ge ratio is about 1 : 1 in the small

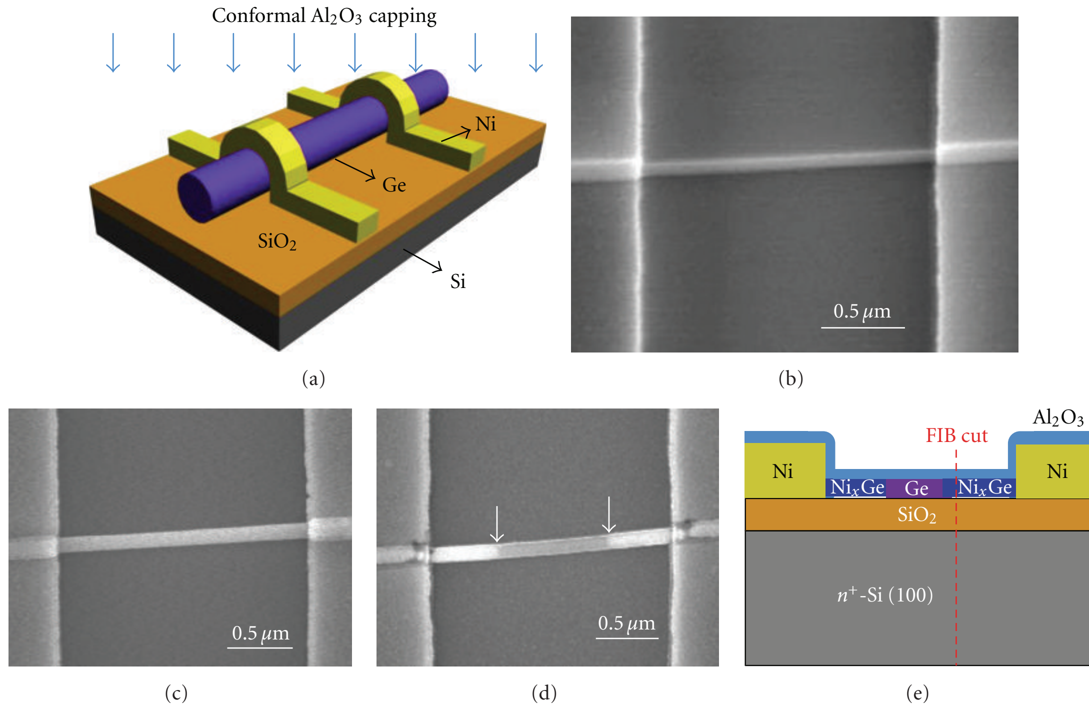

Figure 5: Formation of $Ni_xGe/Ge/Ni_xGe$ heterostructure with the Al_2O_3 confinement. (a) Schematic illustration of an Al_2O_3 conformal capping on the Ge nanowire device by ALD. (b) SEM image of the as-fabricated Ge nanowire device with EBL-defined Ni electrodes. (c) SEM image of the Ge nanowire device after a conformal capping of 20 nm thick Al_2O_3. (d) SEM image of the $Ni_xGe/Ge/Ni_xGe$ heterostructure after RTA at 450°C for 20 s in which the length of the Ge region was easily controlled to be several hundred nanometers. The arrows indicate the growth tip of the Ni_xGe nanowire. (e) Schematic illustration showing the formation of $Ni_xGe/Ge/Ni_xGe$ nanowire heterostructure with the Al_2O_3 confinement. The red line indicates the position chosen for FIB to study the cross-sectional structure in Figure 6. Reproduced from [14].

germanide region close to the Ni_xGe/Ge interface, suggesting the formation of NiGe. This result is consistent with the line-scan profile in Figures 6(d) and 6(e). The length of the NiGe region can range from tens of nanometers to hundreds of nanometers in our experiments. On the other hand, the Ni/Ge ratio is about 2 : 1 in the other germanide region close to the Ni pad on the left, implying that the phase is Ni_2Ge. It is also worth noting that the almost constant concentration of Ge along the heterostructure suggests Ni is the dominant diffusion species in this system [28]. Figure 7(d) shows the lattice-resolved HRTEM image of the Ni_xGe/Ge heterostructure, clearly exhibiting two interfaces. The FFT patterns at the Ni_2Ge, NiGe, and Ge regions are shown in Figures 7(e)–7(g), which help further confirm the germanide phases. The crystallographic epitaxial relationships between the Ge/NiGe interface were determined to be Ge$[01\bar{1}]$//NiGe[010] and Ge$(1\bar{1}\bar{1})$//NiGe(001), while those for the Ni_2Ge/NiGe interface were $Ni_2Ge[100]$//NiGe[010] and $Ni_2Ge(011)$//NiGe(001). It is worth noting that a large lattice mismatch of 77.7% observed at the NiGe/Ge epitaxial interface could result in the segregation of nanoparticles (see Figure 6). In contrast, the epitaxial relationships in the $Ni_2Ge/Ge/Ni_2Ge$ nanowire heterostructure formed without oxide confinement during annealing were found to be Ge$[01\bar{1}]$//$Ni_2Ge[0\bar{1}1]$ and Ge$(1\bar{1}\bar{1})$//$Ni_2Ge(100)$, as we discussed [13]. Therefore, the Al_2O_3 capping layer plays an important role in confining the growth of germanides and also promoting the formation of NiGe to maintain high-quality epitaxial relationships between Ni_2Ge and Ge.

Figure 8 schematically illustrates the epitaxial relationships of the Ni_2Ge/Ge interface in the $Ni_2Ge/Ge/Ni_2Ge$ nanowire heterostructure and the NiGe/Ge interface in the $Ni_2Ge/NiGe/Ge/NiGe/Ni_2Ge$ nanowire heterostructure. According to the epitaxial relationships in both cases, the nanowire growth direction (along the Ge [111] direction) is not perpendicular to the epitaxial planes (parallel to the Ge $(1\bar{1}\bar{1})$ plane). This "twisted" growth mode of nanowires is substantially different from that in the typical epitaxial growth of thin films, in which the growth direction is usually perpendicular to the epitaxial planes [31]. The presence of the oxide capping may alter the energy of the growth and thus change the twisted angle. Furthermore, it suggests that the twisting in nanowires may be used to accommodate substantially large lattice mismatches. This unique growth mode may be attributed to the fact in minimizing the total system energy in the presence of a large lattice mismatch in the interface. Further microscopic studies in simulation and experiment are required to understand the growth kinetics for this unique growth mode in one-dimensional systems.

The formed atomically sharp interface in the $Ni_xGe/Ge/Ni_xGe$ nanowire heterostructures (both with and without Al_2O_3 capping during annealing) can be used

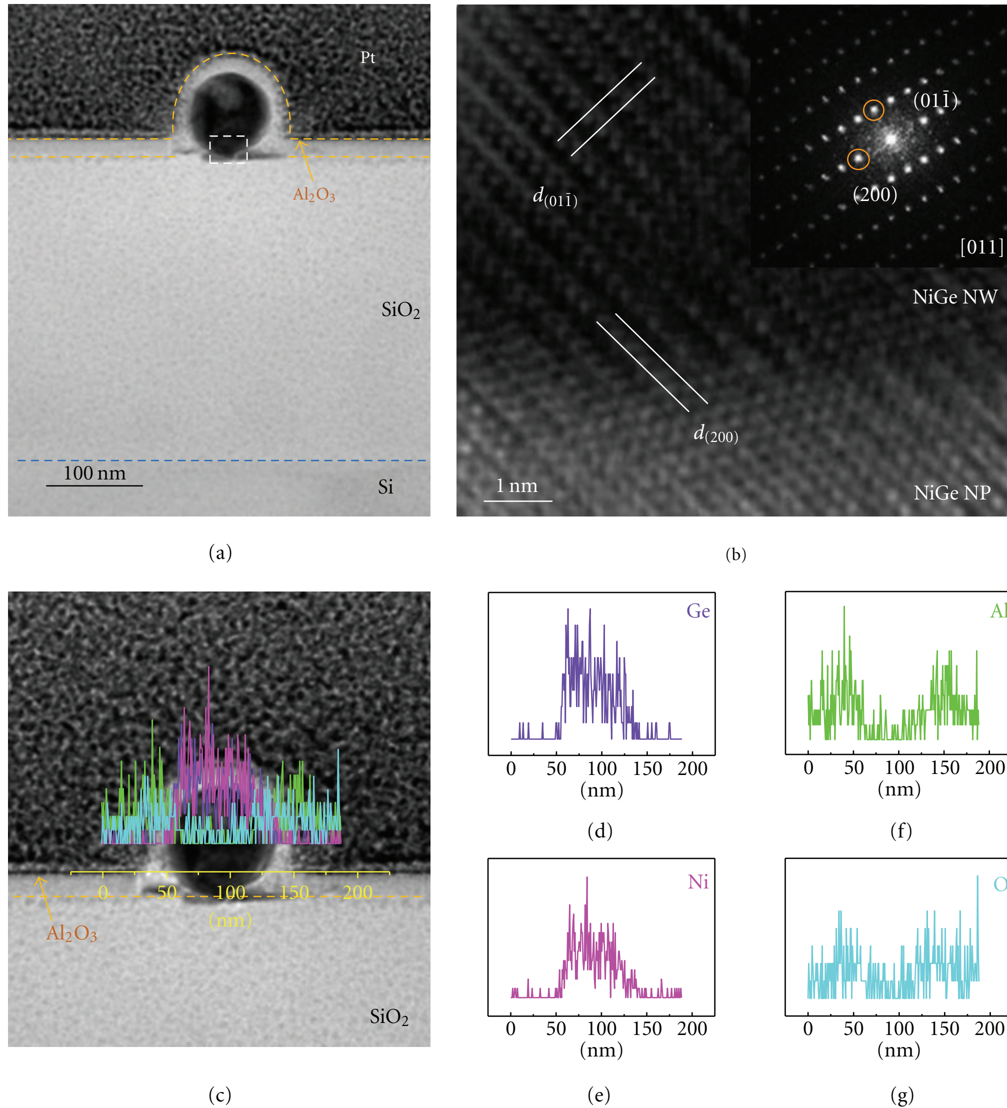

FIGURE 6: Cross-sectional TEM study of a Ni-Ge nanowire device on a SiO_2/Si substrate cut with FIB. (a) Low-magnification cross-sectional TEM image of the NiGe region. The 20 nm thick Al_2O_3 film provides a conformal capping on the device surface and germanide nanoparticles are clearly observed as they segregated underneath the nanowire, the region that is not covered by Al_2O_3. (b) Lattice-resolved HRTEM image of the interface between the formed NiGe nanowire (NW) and the segregated NiGe nanoparticle (NP), as indicated by the white rectangle in Figure 5(a). The inset shows the corresponding FFT pattern. The labeled lattice spacings for NiGe are: $d_{(01\text{-}1)} = 0.295$ nm and $d_{(200)} = 0.269$ nm. (c) Cross-sectional TEM image with the line-scan profiles of Ge, Ni, Al and O atoms. (d)–(g) The individual line-scan profile of Ge, Ni, Al, and O atoms, respectively, The Ni/Ge ratio is about 1 : 1. Reproduced from [14].

to explore promising applications in nanoscale devices [6, 7, 10, 16]. As aforementioned, this Ni_xGe/Ge/Ni_xGe nanowire heterostructure can be easily used to fabricate Ge nanowire FETs, in which the germanide regions Ni_xGe can be used as source/drain contacts to the Ge nanowire channel. The channel length can be simply controlled by the annealing time and growth length of the germanide nanowire; therefore, it can be well controlled to sub-100 nm using a convenient RTA process. Clearly, this simple process has a great advantage over traditional complex and expensive photolithography technology in achieving short-channel transistors.

Back-gate FETs were fabricated on the SiO_2/Si substrate to study the electrical transport property of the Ni_2Ge/Ge/Ni_2Ge nanowire heterostructure. The Si substrate is degenerately doped to serve as a back gate. The device schematic is shown in Figure 9(a), and electrical measurements were performed using a probe station with a Keithley 4200 semiconductor parameter analyzer. For comparison, Figure 9(b) shows the logarithm plot of typical I_{ds}-V_{gs} curves for the Ge nanowire FET at various drain voltages before and after RTA. They both show a p-type transistor behavior, although we intended to grow undoped Ge nanowires. This is mainly due to the Fermi level pinning at the Ge nanowire

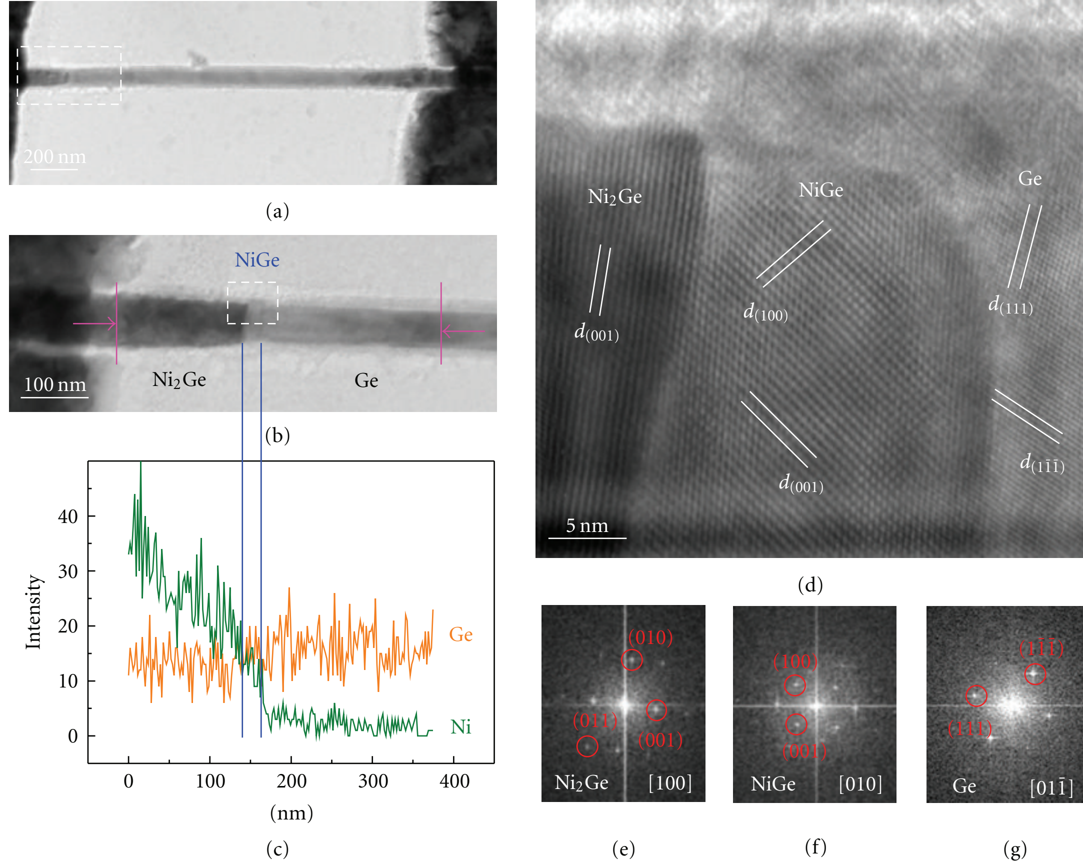

FIGURE 7: Plane-view TEM images of Ni-Ge nanowire devices on a TEM grid with a 50 nm thick Si_3N_4 window. (a) Low-magnification TEM image of a Ge nanowire reacted with 120 nm thick Ni pads upon 450°C RTA for 30 s. (b) Enlarged TEM image from the white rectangle in (a). These regions with different contrasts and compositions are labeled. (c) Corresponding EDS line-scan profiles of Ge and Ni across the region between two red lines in (b). (d) Lattice-resolved TEM image of the formed Ni_xGe/Ge nanowire heterostructure from the white rectangle in (b). The labeled lattice spacings are: $d_{(001)} = 0.5036$ nm for Ni_2Ge; $d_{(100)} = 0.538$ nm and $d_{(001)} = 0.5811$ nm for NiGe; $d_{(111)} = 0.3265$ nm and $d_{(1\text{-}1\text{-}1)} = 0.3265$ nm for Ge. (e)–(g) are the FFT patterns taken from the Ni_2Ge, NiGe, and Ge regions in (d), respectively. Reproduced from [14].

surface induced by Ge surface states, which tends to result in hole accumulation [26, 27]. The maximum current measured before RTA at $V_{ds} = 0.5$ V is about 30 nA, corresponding to a current density of 2.4×10^3 A/cm^2. The current density is relatively small due to a large Schottky barrier at the source/drain contacts before annealing. To extract the mobility, we first used the cylinder-on-plate model to estimate the gate capacitance coupling between the Ge nanowire and the back-gate oxide as

$$C_{ox} = \frac{2\pi\varepsilon_{ox}\varepsilon_0 L}{\cosh^{-1}((r + t_{ox})/r)}, \quad (1)$$

(see [32]) where $\varepsilon_0 = 8.85 \times 10^{-14}$ F/cm is the vacuum dielectric constant, $\varepsilon_{ox} = 3.9$ is the relative dielectric constant for SiO_2, and $r = 20$ nm is the radius of the Ge nanowire. The Ge nanowire channel bis $L = 3\,\mu$m, and the thickness of the back-gate dielectric is $t_{ox} = 330$ nm. Given the above parameters, the estimated gate capacitance is $C_{ox} = 1.83 \times 10^{-16}$ F. The field effect hole mobility can be extracted from the I_{ds}-V_{gs} curves using the transconductance (g_m) at a fixed drain bias V_{ds}

$$\mu = \frac{g_m L^2}{V_{ds} C_{ox}}. \quad (2)$$

Using the maximum transconductance extracted from the I_{ds}-V_{gs} curves, the hole mobility obtained falls in the range of 3–8 cm^2/Vs. This is consistent with previous reported values (less than 10 cm^2/Vs) for SFLS-synthesized Ge nanowires [25].

After RTA at 400°C for 15 s, however, electrical transport measurements on the Ge nanowire device show much improved transistor characteristics, as shown in Figure 9(b). The gate bias was scanned from 0 V to −40 V, the latter of which corresponds to a maximum vertical gate electrical field of 1.21×10^6 V/cm. The I_{ds}-V_{gs} curves show a p-type behavior with an on/off ratio larger than 10^3. The maximum current measured at $V_{ds} = 0.5$ V is about 0.7 μA corresponding to a current density of 5.6×10^4 A/cm^2, which was more than 20 times larger after annealing, in

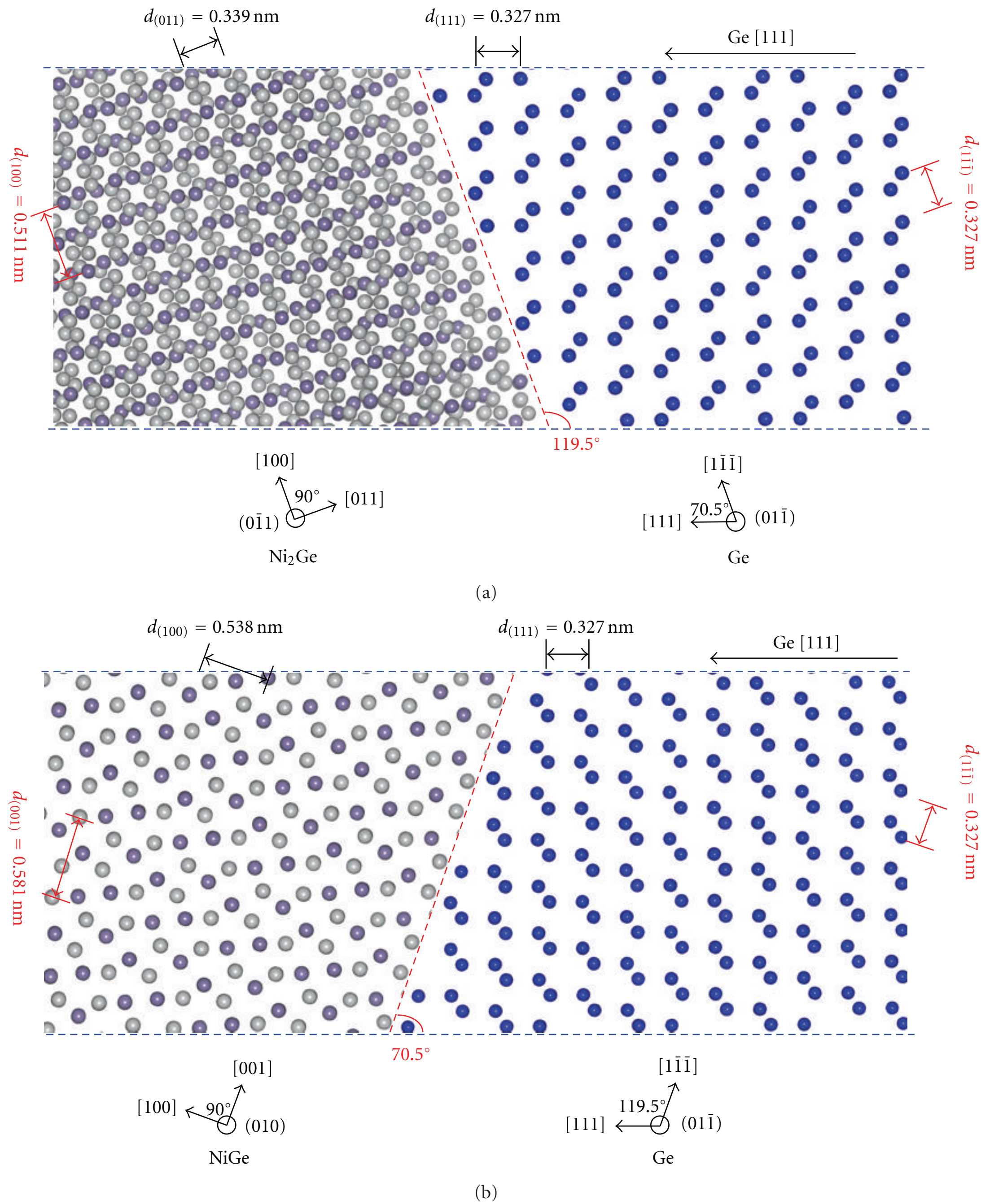

FIGURE 8: Schematic illustration of the epitaxial relationships of (a) the Ni_2Ge/Ge interface in the Ni_2Ge/Ge/Ni_2Ge nanowire heterostructure and (b) the NiGe/Ge interface in the Ni_2Ge/NiGe/Ge/NiGe/Ni_2Ge nanowire heterostructure, respectively. Both of them show "twisted" but different growth modes. The grey and purple balls represent the Ni and Ge atoms in the Ni_xGe lattice, respectively, while the blue one represents the Ge atom in the Ge lattice. Reproduced from [14].

which the Ni_2Ge contact to the Ge nanowire channel was developed. The maximum transconductance extracted from I_{ds}-V_{gs} curves at drain bias V_{ds} = 0.1 V is 13.3 nS, giving rise to a field-effect hole mobility of 65.2 cm^2/Vs. Although this mobility is still lower than the reported value from VLS-grown Ge nanowires [14, 16], it still shows about one order of magnitude improvement among SFLS-synthesized Ge nanowires [25], and this increase may be attributed to the atomically sharp contact of Ni_2Ge to the Ge nanowire.

Similarly, the Ni_2Ge/NiGe/Ge/NiGe/Ni_2Ge nanowire heterostructures formed with Al_2O_3 capping during annealing can also be used to fabricate Ge nanowire FETs. To further improve the transistor performance, VLS-grown nanowires were used in this study because of their higher

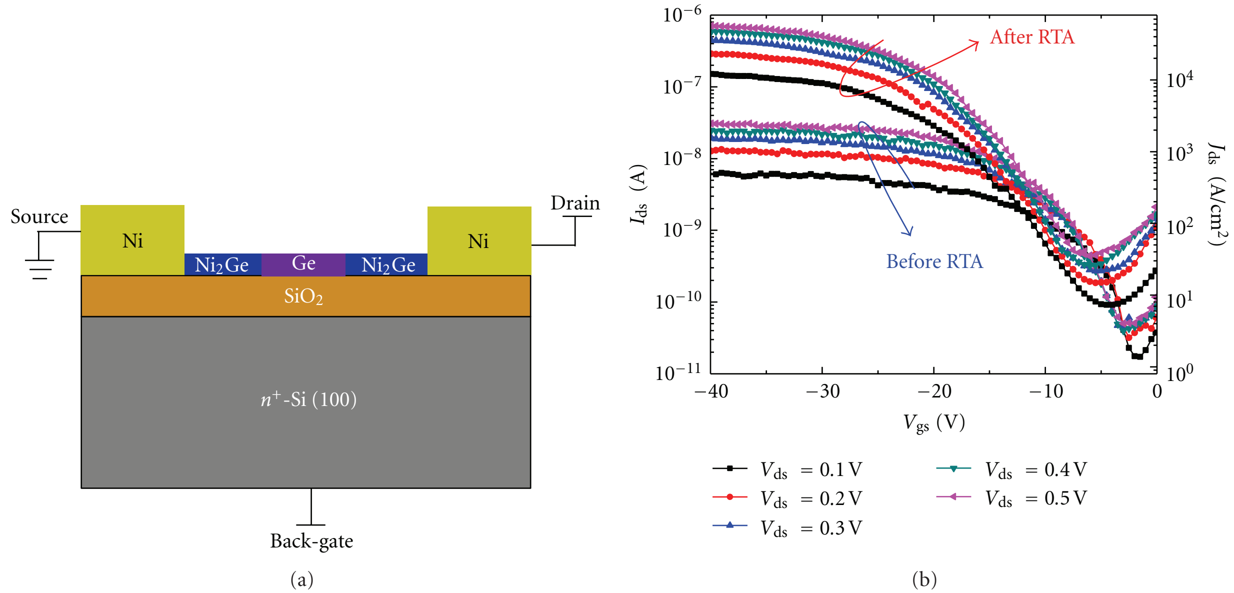

FIGURE 9: Electrical characterization of Ge nanowire back-gate FETs (without Al_2O_3 capping during annealing) at 300 K. (a) Schematic illustration of a Ge nanowire back-gate FET. (b) I_{ds}-V_{gs} curves of the back-gate Ge nanowire transistor before and after RTA, both showing a p-type MOSFET behavior. The transistor performance was significantly improved after RTA, in which the Ni_2Ge source/drain contacts were formed. Reproduced from [13].

carrier mobility. Back-gate nanowire FETs were fabricated on the SiO_2/Si substrate similarly as shown in Figure 10(a). Figure 10(b) shows the typical I_{ds}-V_{gs} curves of a back-gate Ge nanowire FET after RTA at 450°C for 20 s, in which the on/off ratio is as high as 10^5. The maximum transconductance is obtained to be about 0.168 μS at V_{ds} = 0.1 V, which gives rise to a normalized transconductance of 2.4 μS/μm, assuming the effective channel length is equal to the nanowire diameter (70 nm) [10]. The extracted hole mobility in our experiments is typically in the range of 150–210 cm^2/Vs. Compared with SFLS-synthesized Ge nanowires, the significant improvement in the transistor performance here could be attributed to a better crystalline quality of VLS-grown Ge nanowires. Figure 10(c) shows the typical I_{ds}-V_{ds} curves of a back-gate Ge nanowire FET at various gate voltages.

As explained above, the Al_2O_3 capping layer helps confine the growth of germanide in a Ge nanowire during thermal annealing. More importantly, it is of interest to study the effect of the Al_2O_3 capping layer on the device performance. In the previous study on the metal contacts to Ge substrate through a thin layer of Al_2O_3 tunneling oxide by Zhou et al., it is found that Al_2O_3 helps terminate the dangling bonds and passivate the Ge surface, therefore, alleviate Fermi level pinning effect [12]. In this study, dual sweepings of gate bias in the I_{ds}-V_{gs} curves were performed to investigate the charge trapping due to the Al_2O_3 capping layer on passivating the Ge nanowire surface. Figure 10(d) shows the I_{ds}-V_{gs} curves under various conditions: before Al_2O_3 deposition (both in air and in vacuum) and after Al_2O_3 deposition at 250°C. The gate bias was swept from +40 V to −40 V then back to +40 V in steps of 0.5 V at a fixed drain bias of V_{ds} = 20 mV. The I_{ds}-V_{gs} curve measured in air before annealing shows the biggest hysteresis, which is mainly due to the absorption of molecules from the ambient and the charge trapping on the Ge surface [26, 33]. The measured reduced hysteresis in a vacuum (less than 10^{-5} Torr), however, rules out the contribution from the ambient. Also, measurements in the vacuum help reduce scatterings from the molecules absorbed on the Ge surface as carriers transport along the Ge nanowire channel, which will reduce the resistance of Ge nanowires. Furthermore, the hysteresis was significantly reduced after the Al_2O_3 deposition, which unambiguously demonstrates the passivation effect of the Al_2O_3 layer on the Ge nanowire surface [12]. Besides, the Al_2O_3 passivation could again reduce scatterings for carriers transport along the Ge nanowire channel and thus further reduce the resistance of Ge nanowires. The small hysteresis present after Al_2O_3 passivation, however, may arise from the charge trapping on the Ge surface between the Ge nanowire channel and the back-gate dielectric, the region that is not covered by the Al_2O_3 capping layer.

3. Conclusion and Discussion for Future Study

In summary, Ge nanowire heterostructures with atomically sharp interfaces have been demonstrated by the solid-state reaction between a single-crystalline Ge nanowire and Ni contact pads via a facile rapid thermal annealing process in a temperature range of 400–500°C. The crystallographic epitaxial relationships in the formation of the Ni_2Ge/Ge/Ni_2Ge nanowire heterostructure were determined

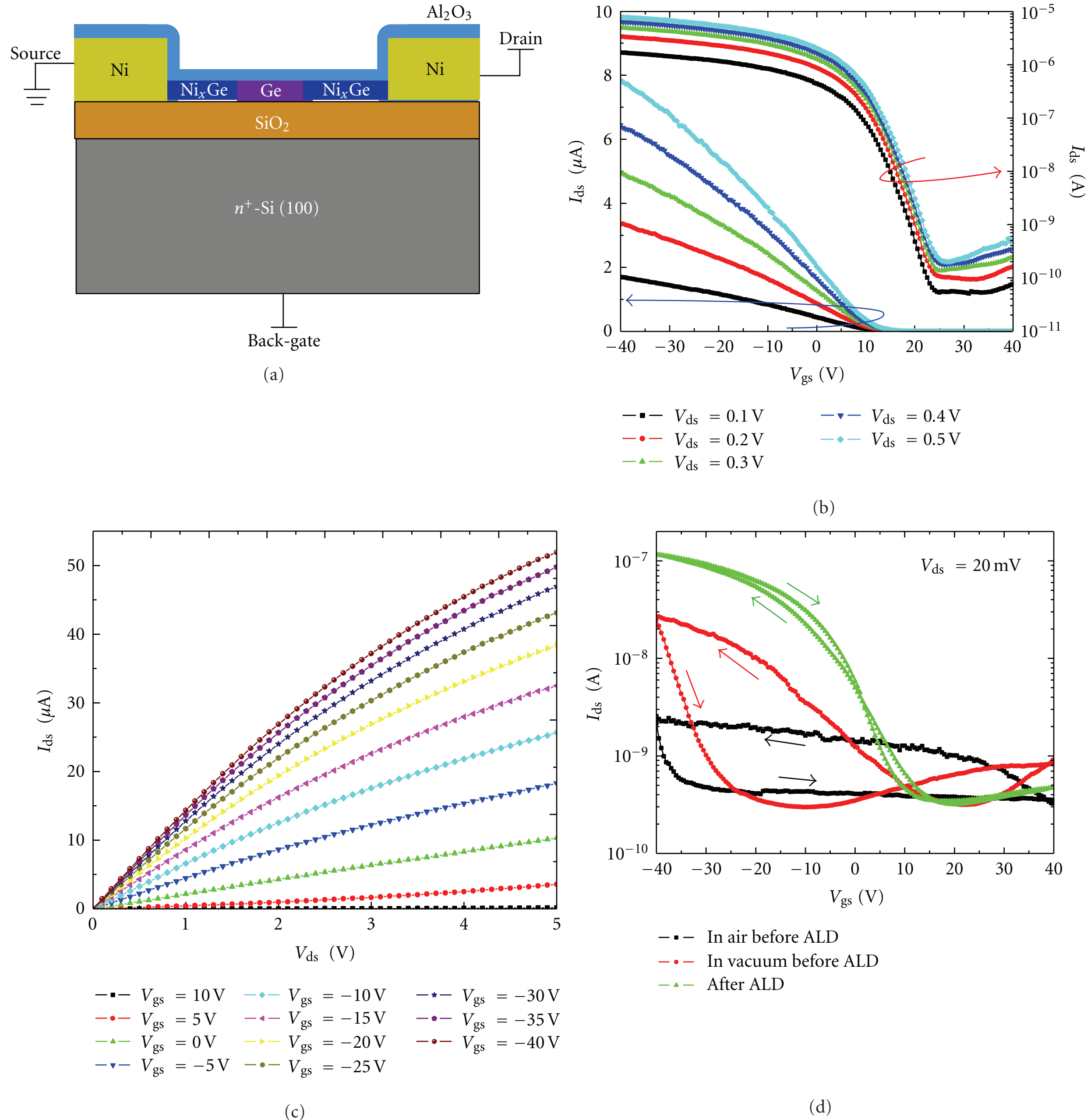

Figure 10: Electrical characteristics of Ge nanowire back-gate FETs (with Al_2O_3 capping during annealing) at 300 K. (a) Schematic illustration of a Ge nanowire back-gate FET. (b) I_{ds}-V_{gs} curves of the back-gate Ge nanowire transistor after RTA, showing a p-type MOSFET behavior. (c) I_{ds}-V_{ds} curves of the back-gate Ge nanowire transistor after RTA. (d) Dual sweepings of the gate bias V_{gs} between +40 V to −40 V showing different sizes of hysteresis under various conditions. The arrows indicate the sweeping directions. The hysteresis was significantly reduced after Al_2O_3 passivation. A small hysteresis was still observed after ALD, which may be attributed to the charge trapping on the Ge surface between the Ge nanowire channel and the back-gate dielectric, the region that is not covered by the Al_2O_3 capping layer. Reproduced from [14].

to be Ge$[01\bar{1}]$//$Ni_2Ge[0\bar{1}1]$ and Ge$(1\bar{1}\,\bar{1})$//$Ni_2Ge(100)$. Back-gate FETs were fabricated using the formed Ni_2Ge region as source/drain contacts to the Ge nanowire channel. The electrical measurement shows an on/off ratio over 10^3 and a field-effect hole mobility of about 65.4 cm^2/Vs, which are superior to reported values for SFLS-synthesized Ge nanowires.

More importantly, the effect of oxide confinement on the formation of the Ge nanowire heterostructure was studied by capping the Ge nanowire device with a layer of Al_2O_3 before the annealing process. In contrast to the single germanide phase in the Ni_2Ge/Ge/Ni_2Ge nanowire heterostructure, a segment of high-quality epitaxial NiGe was then formed between Ni_2Ge and Ge. The crystallographic epitaxial

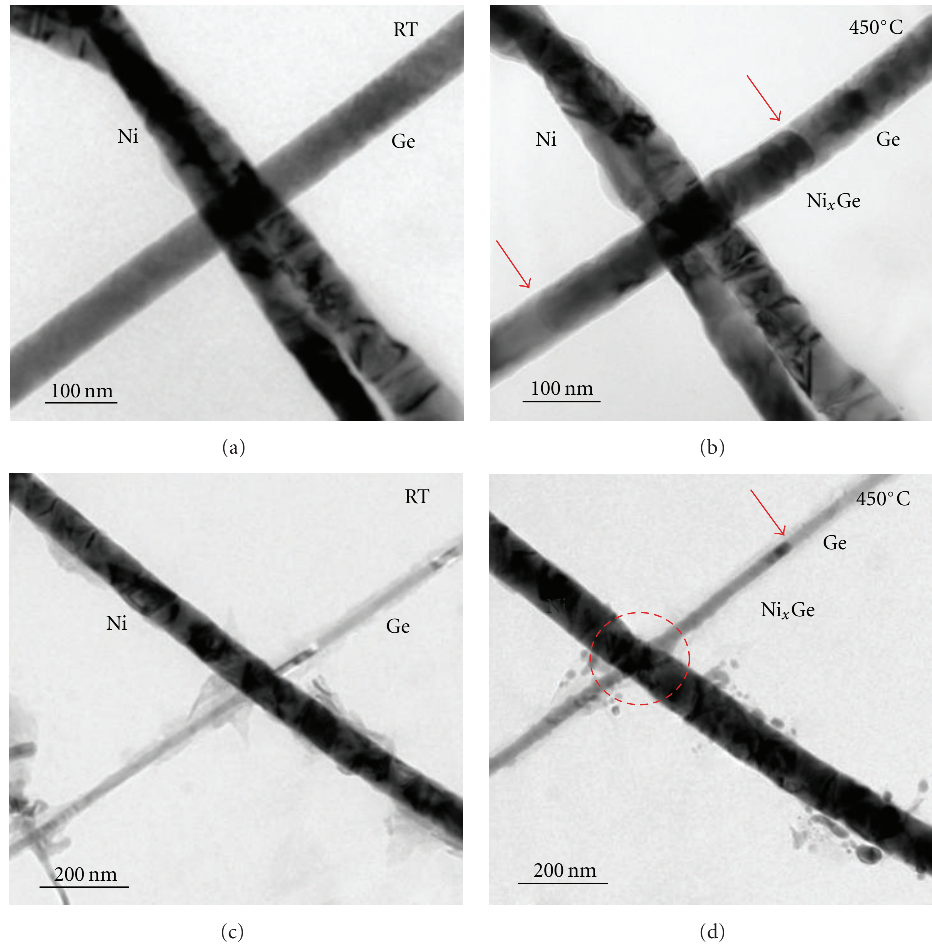

Figure 11: (a) TEM image of a Ge nanowire in point-contact with two Ni nanowires on the TEM grid at room temperature. (b) TEM image showing the diffusion of Ni into the Ge nanowire upon 450°C annealing. The red arrows indicate the growth tip of the Ni_xGe nanowire. (c) TEM image of another Ge nanowire in point contact with a Ni nanowire on the TEM grid at room temperature. (d) TEM image showing the diffusion of Ni into the Ge nanowire upon 450°C annealing. The red circle highlights the consumption of Ni in the formation of the Ni_xGe nanowire upon annealing. Also, the segregation of Ni_xGe nanoparticles was not observed in the Ni-Ge nanowire point-contact system upon annealing.

relationships were determined to be Ge$[01\bar{1}]$//NiGe[010] and Ge$(1\bar{1}\bar{1})$//NiGe(001) for the Ge/NiGe interface and Ni_2Ge[100]//NiGe[010] and Ni_2Ge(011)//NiGe(001) for the Ni_2Ge/NiGe interface, respectively. Similarly, back-gate FETs were fabricated on the formed Ni_2Ge/NiGe/Ge/NiGe/Ni_2Ge nanowire heterostructure, and the electrical measurements reveal a high-performance p-type behavior, showing a high on/off ratio of 10^5 and a field-effect hole mobility of about 210 cm^2/Vs. Moreover, the Al_2O_3 capping was found to passivate the Ge nanowire surface as well as to provide an appreciable confinement during the growth of germanide and changes its composition to maintain the high-quality epitaxial relationships.

For further understanding the growth kinetics of Ge nanowire heterostructures, a more detailed study is required [8, 9, 34–36]. For instance, the size of the metal diffusion (contact) source may affect the formation of Ge nanowire heterostructure, especially the segregation of nanoparticles. In this paper, the metal source was defined with EBL and e-beam evaporation, in which the size of planar Ni contacts (typically in the μm range) is much larger than the diameter of Ge nanowires (typically below 100 nm) [13]. On the other hand, in some other studies of Si nanowire heterostructures, another extensively-studied diffusion source was metal nanowires or dots (refer to Table 1), which led to a point-contact rather than a planar contact to the Si nanowire [8, 9, 37, 38]. Similarly, we have also studied the formation of Ge nanowire heterostructures through the point contact reaction between a Ge nanowire and a Ni nanowire. Figure 11(a) shows the TEM image of a Ge nanowire in point contact with two Ni nanowires on the TEM grid at room temperature. The Ni nanowires were prepared by the electrochemical deposition, and the diameter was typically 50–100 nm which depends on the size of the anodic aluminum oxide (AAO) template. Figure 11(b) shows the TEM image, similarly illustrating the diffusion

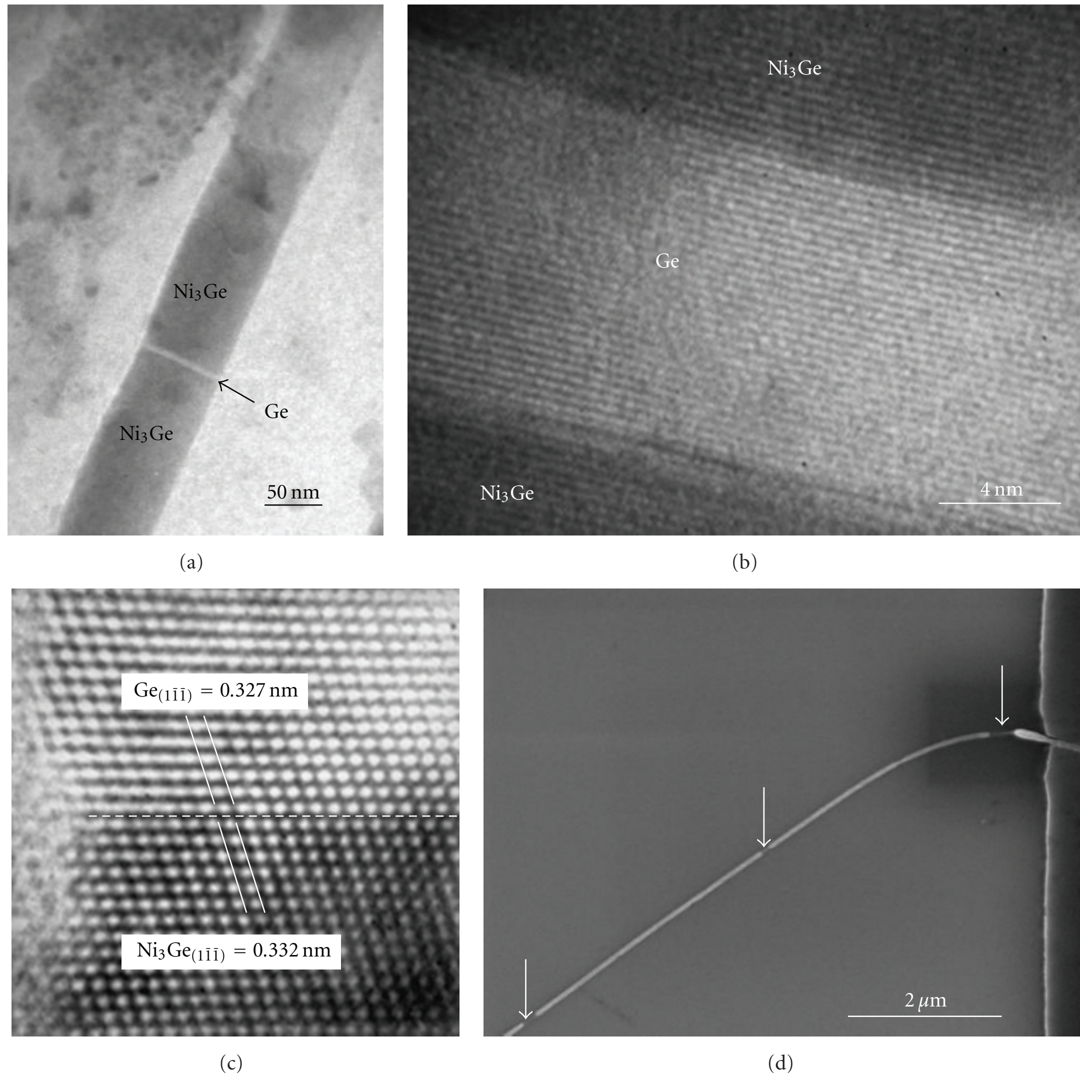

FIGURE 12: (a) TEM image of a fragmented Ni_3Ge nanowire on the TEM grid upon 650°C annealing. (b) HRTEM image of the Ni_3Ge/Ge/Ni_3Ge nanowire heterostructure showing a clean and sharp interface. (c) Lattice-resolved HRTEM image of the Ni_3Ge/Ge interface. The measured lattice mismatch was only 1.5% at the $Ni_3Ge(1\bar{1}\bar{1})$/$Ge(1\bar{1}\bar{1})$ interface. As a result, the twisted growth mode, which was observed in both Ni_2Ge/Ge/Ni_2Ge and Ni_2Ge/NiGe/Ge/NiGe/Ni_2Ge nanowire heterostructures to accommodate the large lattice mismatch, did not occur in this Ni_3Ge/Ge/Ni_3Ge nanowire heterostructure. (d) SEM image showing a broken Ge nanowire upon 650°C RTA due to a low melting pointing of the Ge nanowire. Reproduced from [13].

of Ni into the Ge nanowire upon 450°C annealing. The red arrows indicate the growth tip of the Ni_xGe nanowire. It is worth noting that the growth of the Ni_xGe nanowire started from the point-contact region, similar to the planar contact case [13]. However, this is different from the case of the NiSi/Si/NiSi nanowire heterostructure formed via the point-contact reaction between a Si nanowire and a Ni nanowire, in which the growth of NiSi actually started from both ends of the Si nanowire instead of the point-contact region [8]. Further kinetics study is needed to understand the different phenomena in Ge and Si nanowire heterostructures. Figure 11(c) TEM image of another Ge nanowire in point-contact with a Ni nanowire at room temperature. Figure 11(d) shows the TEM image illustrating the diffusion of Ni into the Ge nanowire upon 450°C annealing. Clear consumption of Ni in the formation of the Ni_xGe nanowire upon annealing was observed, as highlighted by the red circle. Moreover, it is surprising that the segregation of Ni_xGe nanoparticles was not observed in the Ni-Ge nanowire point-contact system upon annealing [13]. We believe that the much smaller Ni flux through such point contact compared with the planar contact may play an important role in preventing the segregation of nanoparticles. Therefore, the difference of various metal contacts in the formation of Ge nanowire heterostructures requires further study.

For the device applications, we have demonstrated in this study that the formed germanides with atomically sharp interface to Ge can be used as a good electrical contact.

Indeed, Lin et al. [11] have successfully detected the electrical spin injection into a Si nanowire from the ferromagnetic MnSi contact in the formed MnSi/Si/MnSi nanowire heterostructure. However, the signal can be observed only at relatively low temperature, since MnSi has a low Curie temperature of about 30 K. On the other hand, there are many germanides, such as Mn_5Ge_3 and Ni_3Ge, which exhibit room-temperature ferromagnetism [20, 21], and thus offer great advantages over silicides for promising applications in room-temperature spintronics, including spin injection, transport and detection.

In fact, a room-temperature ferromagnetic germanide phase, Ni_3Ge [20], was developed at high reaction temperature, in which a high-concentration Ni vapor from a large-area Ni contact pattern surrounded the Ge NWs to form a fragmented Ni_3Ge nanowire. Figure 12(a) shows the TEM image of the formed $Ni_3Ge/Ge/Ni_3Ge$ nanowire heterostructure on the TEM grid upon 650°C annealing. Figure 12(b) illustrates the HRTEM image of the Ge nanowire heterostructure with a clean and sharp interface between Ni_3Ge and Ge. The Ge region was controlled down to as small as 12 nm. The strained short Ge region in the $Ni_3Ge/Ge/Ni_3Ge$ nanowire heterostructure is promising for high-performance FETs and spintronics applications [11, 39]. Figure 12(c) shows the lattice-resolved TEM image of the Ni_3Ge-Ge interface, and the formed germanide was identified to be single-crystalline Ni_3Ge with a face-centered cubic (FCC) lattice structure (Fd3m, space group 227 and JCPDS no. 65-7680) and a lattice constant of $a = 0.574$ nm. Although a slight volume expansion was still observed, the Ni_3Ge lattice was well fit with the Ge lattice, due to their same lattice structure and a very small lattice mismatch of only 1.5% (the lattice constant of Ge is $a = 0.568$ nm). It is worth mentioning that the twisted growth mode, which was observed in both $Ni_2Ge/Ge/Ni_2Ge$ and $Ni_2Ge/NiGe/Ge/NiGe/Ni_2Ge$ nanowire heterostructures to accommodate the large lattice mismatch, did not occur in this $Ni_3Ge/Ge/Ni_3Ge$ nanowire heterostructure due to such a small lattice mismatch. However, as mentioned above, the melting point of Ge nanowires is significantly reduced from that of bulk Ge [29]. As a result, Ge nanowires were easily broken at high temperature, as shown in Figure 12(d). Therefore, a ferromagnetic germanide remains undeveloped at a relatively low temperature in order to study the spin transport in Ge nanowire.

Acknowledgments

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